

Introduction

10GbE is a commonly used protocol both for data transmission over long distances as well as embedded communication such as high speed backplanes. A 10GbE MAC is required for both applications, however the 'fully featured' MAC designed to operate over long distances is often overly complicated and too large for short haul backplane applications.

The 10 GbE MAC Lite is a small, easy to use MAC for non line-side, non-managed “local” 10 GbE connections. It instantiates the Altera XAUI Hard IP, so implements the path from the FPGA fabric Avalon-ST packet interface to XAUI.

Features

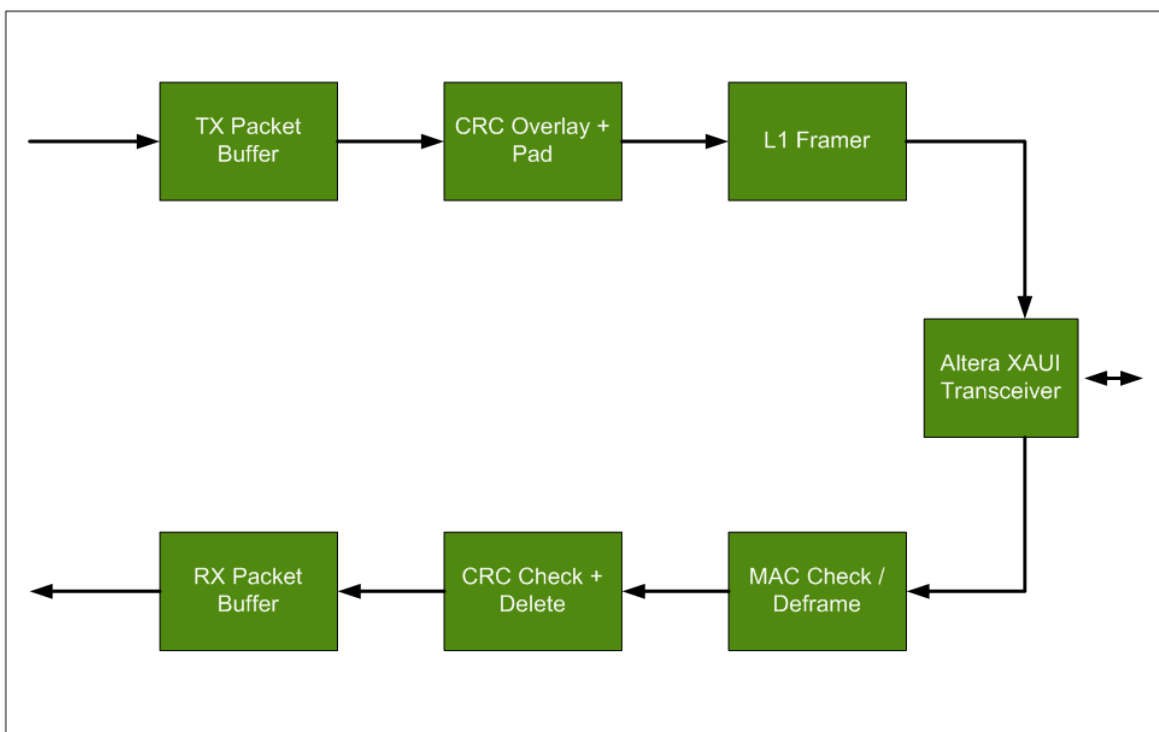
Transmit:

- 64-bit Avalon-ST interface
- Parameterizable packet buffer with “almost full” indication for back pressure
- Automatic padding for undersized packets
- CRC Calculation and Insertion

- L1 Framing
 - SOP + Preamble insertion
 - EOP Insertion
 - IPG insertion with Deficit Idle Counter
- Interface to Altera XAUI PCS Hard IP
- Packet and Byte counters through 32-bit Avalon-MM interface

Receive:

- Interface to Altera XAUI PCS Hard IP
- Deframer and error checking with error counters
 - Fragment, Oversized packet, Undersized packet, and Bit Error counters
- CRC Checking and removal with CRC Error counter
- Parameterizable packet buffer with packet drop on error or when full
 - Packet drops due to buffer full are counted
 - Received good packets and bytes are counted
- All counters are read through 32-bit Avalon-MM interface



Implementation summary

Altera FPGA Implementation summary

Core specifics		
Supported	Stratix2 GX FPGAs and larger	
Resources used		
	Typ	
ALUT's	1,353	
Registers	1,149	
RAM	41 M9K + 32K RX / TX buffers	
Supported Design Tools		
Altera Tool	Quartus II 9.1 or later	
Speed Grade		
All speed grades		

Deliverables

- Design Documentation
- Full Verilog source code
- Simulation Results
 - ModelSim AE Wave file (.wmf file) with all signals logged
 - 10 TX Packets of varying size from Fabric to XAUI
 - 10 RX Packets of varying size from XAUI to Fabric

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